

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
6 October 2005 (06.10.2005)

PCT

(10) International Publication Number
WO 2005/094016 A3

(51) International Patent Classification⁷: **G06F 17/50**

(21) International Application Number:
PCT/US2005/003590

(22) International Filing Date: 2 February 2005 (02.02.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/789,187 27 February 2004 (27.02.2004) US

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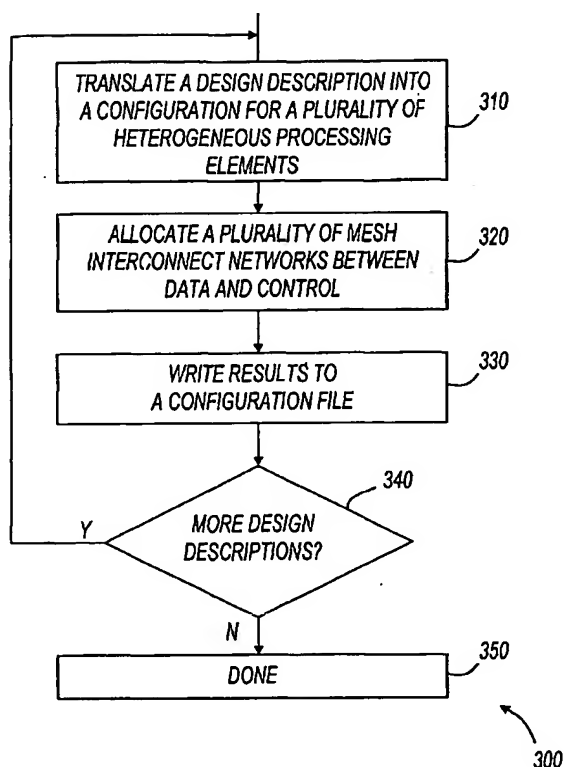
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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,

[Continued on next page]

(54) Title: **ALLOCATION OF COMBINED OR SEPARATED DATA AND CONTROL MESH INTERCONNECT NETWORKS**



(57) Abstract: A dual mesh interconnect network in a heterogeneous configurable circuit may be allocated between data communication and control communication.

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WO 2005/094016 A3



ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(88) Date of publication of the international search report:
8 December 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/003590

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ALBANESI M G ET AL: "A VLSI 128-processor chip for multiresolution image processing" MASSIVELY PARALLEL COMPUTING SYSTEMS, 1994., PROCEEDINGS OF THE FIRST INTERNATIONAL CONFERENCE ON ISCHIA, ITALY 2-6 MAY 1994, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, 2 May 1994 (1994-05-02), pages 296-307, XP010125887 ISBN: 0-8186-6322-7 abstract	1,2,5-7, 9-11,14, 15,17, 21-23, 27,28
Y	page 296 - page 299 figures 2,4 ----- -/--	3,4,12, 18-20, 24-26, 29,30

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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- *G* document member of the same patent family

Date of the actual completion of the international search

16 September 2005

Date of mailing of the international search report

07/10/2005

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/003590

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	HUI ZHANG ET AL: "Interconnect architecture exploration for low-energy reconfigurable single-chip DSPs" VLSI '99. PROCEEDINGS. IEEE COMPUTER SOCIETY WORKSHOP ON ORLANDO, FL, USA 8-9 APRIL 1999, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 8 April 1999 (1999-04-08), pages 2-8, XP010330307 ISBN: 0-7695-0152-4	1,2,5-7, 9-11,14, 15,17, 21-23, 27,28
A	abstract	3,4,12, 18-20, 24-26, 29,30
	page 2 - page 7 figures 1,7,9,11	
Y	----- MARESCAUX T ET AL: "Networks on chip as hardware components of an OS for reconfigurable systems" FIELD-PROGRAMMABLE LOGIC AND APPLICATIONS. 13TH INTERNATIONAL CONFERENCE, FPL 2003. PROCEEDINGS (LECTURE NOTES IN COMPUT. SCI. VOL.2778) SPRINGER-VERLAG BERLIN, GERMANY, 2003, pages 595-605, XP002345294 ISBN: 3-540-40822-3 page 595 - page 596 page 598 - page 603	3,4,12, 18-20, 24-26, 29,30
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	column 10 - column 11 figures 15-18 -----	

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2005/003590

Patent document cited in search report	Publication date	Patent family member(s)	Publication date	
US 6226735	B1	01-05-2001	US 2001029515 A1	11-10-2001

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